# HIGH DENSITY POWER DEVICE FABRICATION PROCESS AND STRUCTURE

## Abstract of the Disclosure

A recessed gate power MOSFET is formed on a substrate (20) including a P-body layer (26), N-drain layer (24) and optional P+ layer (22) for IGBT. A trenching protective layer (30) formed on the substrate upper surface (28) is patterned to define exposed areas (46) as stripes or a matrix, and protected areas. Sidewall spacers (44) of predetermined thickness (52) with inner surfaces (48) contact the protective layer sidewalls. A first trench (50) is formed in substrate areas (46) with sidewalls aligned to the sidewall spacer outer surfaces (47) and extending depthwise through the P-body layer (26) to at least a predetermined depth (56). Gate oxide (60) is formed on the trench walls and gate polysilicon (62) refills the trench to a level (64) near substrate upper surface (28). Oxide (68) between sidewall spacers (44) covers polysilicon (62). Removing the protective layer exposes upper substrate surface (28') between spacer inner surfaces (48). This area is doped to form a source layer (72) atop the body layer (26') and then trenched to form a second trench (80) having sidewalls aligned to the spacer inner surfaces. Second trench (80) defines vertically-oriented source and body layers (86, 90) stacked along gate oxide layer (60) to form vertical channels on opposite sides of second trench (80). Layers (86, 90) have a lateral thickness (88) established by the predetermined spacing of the inner and outer surfaces of the sidewall spacers. Source conductor (94) in the second trench contacts the N-source and P-body layers, and an enhanced P+ region at the base of the second trench.